



SRI VASAVI INSTITUTE OF ENGINEERING & TECHNOLOGY

An Autonomous Institute

(Approved by AICTE, New Delhi & Permanently Affiliated to JNTUK Kakinada)
Accredited by NBA (Mech, ECE, CSE) & NAAC, An ISO 9001:2015 Certified Institute
Nandamuru, Pedana Mandal, Krishna Dist – 521369.



Date : 19-06-2024

M.TECH II SEMESTER (R23 REGULATION) II MID EXAMINATIONS, JULY - 2024

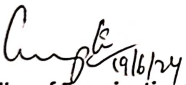
TIME TABLE

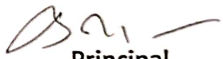
TIME : 10.00 AM TO 12.00 AM

BRANCH	08-07-2024 (MONDAY)	09-07-2024 (TUESDAY)	10-07-2024 (WEDNESDAY)	11-07-2024 (THURSDAY)
ECE (VLSI System Design - 61)	MIXED SIGNAL DESIGN & RF IC DESIGN (M23EC21)	PHYSICAL DESIGN AUTOMATION (M23EC22)	Elective – III DESIGN FOR TESTABILITY (M23EC23A)	Elective – IV LOW POWER VLSI DESIGN (M23EC24C)

NOTE:

- Any Omissions or clashes in this time table may please be informed to the controller of examination immediately.
- The HOD's are requested to inform the Controller of Examination any other substitute subjects that are not included in the above time table immediately.


Controller of Examinations


Principal

Copy to:

- Chairman, Secretary, Correspondent,
- Executive Directors,
- Controller of Examinations,
- Hod – ECE,
- Main Notice Board, Student's Notice Board, Circular file & Exam Cell